UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,248	09/12/2003	Lawrence John Varnerin III	INTECH 3 . 0-012	8691

530 7590 05/04/2005

LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK
600 SOUTH AVENUE WEST
WESTFIELD, NJ 07090

EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,248	VARNERIN ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/12/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Objections

2. Claim 34 objected to because of the following informalities: "dielectric" should apparently be -- nitride dielectric --, otherwise the term "nitride dielectric" in claim 36 would lack the proper antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 9-11, 17, 20-25, 27-28, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Shih et al. (U.S. Patent No. 6,020,263).

5. As to claim 1, Shih discloses a method of processing a semiconductor wafer comprising the steps of: (a) providing a wafer having a planar top surface defined by a layer of a first material (12) with elements of a second material embedded therein

(32/34) (column 4, lines 47-55; Figures 7A-7B); (b) etching at least a portion of said top surface with an etchant which preferentially attacks said first material (12) so as form a new top surface with said elements of said second material (32/34) protruding from surrounding portions of said new top surface (column 5, lines 4-14); and (c) optically locating one or more raised features on said wafer defined by said protruding second material elements or overlying said protruding second material elements (column 5, lines 14-18; lines 27-34).

6. As to claim 2, Shih discloses that said step of depositing one or more additional layers on said new top surface before said locating step (column 5, lines 14-18).

7. As to claim 3, Shih discloses that said step of optically locating said raised features includes directing light through one or more of said additional layers to said raised features and detecting light which has interacted with said raised features (column 5, lines 27-44).

8. As to claim 4, Shih discloses that said step of depositing one or more additional layers (25) includes depositing an opaque lower additional layer of substantially uniform thickness so that said lower additional layer defines an upper surface having said raised features overlying the protruding second material elements (column 5, lines 14-18; Figure 9).

9. As to claim 5, Shih discloses that said step of depositing one or more additional layers includes the step of depositing one or more transparent layers (24) over said upper surface of said opaque lower additional layer (25) (column 5, lines 14-18), and wherein said step of directing light includes directing light through said one or more

transparent layers to said raised features at said upper surface (column 5, lines 27-44). Although Shih does not expressly disclose that photoresist is transparent, Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press (1986), is cited to show that photoresist is inherently transparent to light waves (pages 438-439).

10. As to claim 6, Shih discloses that said protruding second material elements project above the surrounding portions of said new top surface by a protrusion height of less than about 100 nm (column 5, lines 4-8).

11. As to claim 9, Shih discloses that said one or more transparent layers (24) includes a layer of a photoresist (column 5, lines 14-18).

12. As to claim 10, Shih discloses that said lower additional layer (25) is formed from a metallic material (column 5, lines 14-18).

13. As to claim 11, Shih discloses that said second material (32/34) is metallic (column 4, lines 53-54) and said lower layer (25) is deposited directly on said new top surface of said wafer, so that said metallic lower additional layer is contiguous with said elements formed from said second material (column 5, lines 14-18; Figure 9).

14. As to claim 17, Shih discloses that said wafer includes at least one functional region (22) and at least one alignment region (20) (column 4, lines 1-4), said elements formed from said second material include one or more alignment marks (14) (column 4, lines 14-15) disposed in said at least one alignment region (20), and said step of etching said top surface is performed only in said at least one alignment region (column 5, lines 4-9; Figure 8).

15. As to claim 20, Shih discloses that said locating step is performed so as to locate the wafer in the frame of reference of a processing apparatus, the method further comprising forming additional features on the wafer at least in part by operation of said processing apparatus (column 5, lines 27-34).

16. As to claim 21, Shih discloses that said processing apparatus is a wafer stepper and said step of forming additional features includes applying patterned illumination to the wafer (column 5, lines 27-44).

17. As to claim 22, Shih discloses a method of processing a semiconductor wafer comprising the steps of: (a) providing a starting wafer (10) (column 2, line 8) including a top layer of dielectric (12) with metallic damascene elements (32/34) therein, said layer having a planar top surface, said dielectric and said damascene elements being exposed at said top surface (column 4, lines 47-55; Figures 7A-7B); (b) etching said top surface with an etchant which preferentially attacks said dielectric (12) so as to form a new top surface with said damascene elements (32/34) protruding from said dielectric (12) (column 5, lines 4-14); and (c) depositing a metallic layer (25) of substantially uniform thickness on said top surface so that said metallic layer defines an upper surface having raised features overlying said damascene elements projecting (column 5, lines 14-18; column 4, lines 65-67; Figure 9).

18. Although Shih does not expressly use the term "damascene," the reference inherently describes the damascene method. Contact holes (14) and alignment lines (15) are formed in dielectric (12) (column 4, lines 12-13). Metal layers (32/34) are formed over wafer (10) to cover and fill contact holes (14) and alignment lines (15)

(column 4, lines 29-36; Figure 6A-6B). The wafer is planarized to remove the portions of metal layers (32/34) directly above material (12) (column 4, lines 47-52). Wolf, *Silicon Processing for the VLSI Era*, vol. 4, Lattice Press (2002), which is cited to describe the damascene method, describes the damascene process as patterning a via in a dielectric layer, blanket depositing a metal to fill the via, and planarizing the dielectric to form the via plug (page 673, Figure 15-2).

19. As to claim 23, Shih discloses the steps of locating said raised features and registering the wafer with processing apparatus based on the detected locations (column 5, lines 27-44).

20. As to claim 24, Shih discloses the step of depositing a photoresist layer (24) over said metallic layer (25) before said locating step (column 5, lines 14-18), said step of locating including directing light through said photoresist layer (column 5, lines 27-34).

21. As to claim 25, Shih discloses that said step of providing a starting wafer includes chemical mechanical polishing (column 4, lines 47-49).

22. As to claim 27, Shih discloses that said starting wafer includes at least one functional region (22) and at least one alignment region (20) (column 4, lines 1-4), said damascene elements include alignment marks (14) (column 4, lines 14-15) disposed in said at least one alignment region (20) and functional damascene elements in said at least one functional region (22) (column 2, lines 10-13), said step of etching said top surface is performed in said at least one alignment region but not in said at least one functional region (column 5, lines 4-9; Figure 8).

23. As to claim 28, Shih discloses that said dielectric (12) includes SiO_2 at said top surface (column 4, lines 4-5).

24. As to claim 30, Shih discloses that said etching step includes exposing said top surface to an etchant selected from the group consisting of hydrofluoric acid solutions and fluorine-containing plasmas (column 5, lines 9-11).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

27. Claims 8, 18, 26, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shih.

28. As to claim 8, Shih does not expressly disclose that said protrusion height is between about 20 nm and about 50 nm. However, Shih does disclose a lower limit for the of the protrusion height of about 100 nm (column 5, lines 4-6). A protrusion height between about 20 nm and about 50 nm is close enough to a protrusion height of 100 nm, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a protrusion height is between about 20 nm and about 50 nm. One who is skilled in the art would be motivated to select a protrusion height similar to 100 nm, because this height has been successfully shown to successfully produce an alignment marker.

29. As to claim 18, Shih does not expressly disclose that step of etching said top surface is performed over the entire top surface. However, it would have been obvious to one of ordinary skill in the art at to perform a single etching step which etches the entire wafer. One who is skilled in the art would be motivated to reduce the number of processing steps required to form the alignment mark.

30. As to claim 26, Shih does not expressly disclose that said step of etching said top surface includes exposing said damascene features and said dielectric at said top surface to an etchant non-selectively, over the entire top surface of the wafer. However, it would have been obvious to one of ordinary skill in the art at to perform a single etching step which etches the entire wafer. One who is skilled in the art would be motivated to reduce the number of processing steps required to form the alignment mark.

31. As to claim 31, Shih does not expressly disclose that said step of etching said top surface is performed so as to leave said damascene features protruding above said dielectric by 20 to 50 nm. However, Shih does disclose a lower limit for the of the protrusion height of about 100 nm (column 5, lines 4-6). A protrusion height between about 20 nm and about 50 nm is close enough to a protrusion height of 100 nm, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to leave said damascene features protruding above said dielectric by 20 to 50 nm. One who is skilled in the art would be motivated to select a protrusion height similar to 100 nm, because this height has been successfully shown to successfully produce an alignment marker.

32. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of Yu (U.S. Patent No. 5,904,563).

33. As to claim 7, Shih does not expressly disclose that said opaque lower additional layer has a thickness less than about ten times said protrusion height. However, Yu discloses a method of processing a semiconductor wafer comprising the steps of: providing a wafer having a planar top surface defined by a layer of a first material (12) with elements of a second material embedded therein (14) (column 2, lines 23-38); etching at least a portion of said top surface with an etchant which preferentially attacks said first material (12) so as form a new top surface with said elements of said second material (14) protruding from surrounding portions of said new top surface (column 2, lines 1-2; column 3, lines 1-4). Moreover, the second material (14) projects above the surrounding portions of the top surface by a protrusion height of about 100 nm to 140

nm (column 3, lines 8-11). Yu further teaches that the alignment mark is generated by a blanket deposition of conductive layer (21) over the surface to produce an edge with sufficient optical contrast (column 3, lines 12-16). The thickness of conductive layer (21) is between 3,000 Å and 8,000 Å (column 3, lines 18-20), or a thickness less than about ten times the protrusion height. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the lower additional layer with a thickness less than about ten times said protrusion height. One who is skilled in the art would be motivated to form the lower additional layer with a sufficient thickness to produce sufficient optical contrast.

34. Claims 12 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of Wolf, *Silicon Processing for the VLSI Era*, vol. 4, Lattice Press (2002).

35. As to claim 12, Shih not expressly disclose that said second material and said metallic material of said lower layer consist essentially of copper. However, Shih discloses that said second material (32/34) is metallic (column 4, lines 53-54) and that said lower layer (25) is an electrode (column 5, lines 18). Wolf teaches that copper interconnects offer several advantages, including lower resistivity than traditional aluminum interconnects (page 712), greater electromigration characteristics than aluminum (page 716), and manufacturing costs than aluminum (page 718). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form said second material and said metallic material of said lower layer

consist essentially of copper. One who is skilled in the art would be motivated to use copper due to its beneficial characteristics, as taught by Wolf.

36. As to claim 29, Shih not expressly disclose that said damascene features include copper. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form said damascene features to include copper, as discussed above.

37. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shih Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press (1986).

38. As to claim 32, although Shih discloses depositing a photoresist layer (24) over said metallic layer (25) (column 5, lines 14-18) before said locating step said step of locating including directing light through said photoresist layer (column 5, lines 27-38), the reference does not expressly disclose depositing a photoresist layer between 100 nm and 1 μm thick. Wolf teaches that the common thickness of photoresist can vary between 1.5 μm to 0.5 μm, depending upon the spin speed (page 432; Figure 17). It should be noted that there is a substantial overlap between the applicants' thickness range and Wolf's range. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to depositing a photoresist layer between 100 nm and 1 μm thick. One who is skilled in the art would be motivated to select a photoresist thickness similar to a thickness range commonly used.

39. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of Wolf, in further view of Yu.

40. As to claim 33, Shih does not expressly disclose that said metallic layer is less than about 500 nm thick. However, Yu discloses a method of processing a semiconductor wafer comprising the steps of: providing a wafer having a planar top surface defined by a layer of a first material (12) with elements of a second material embedded therein (14) (column 2, lines 23-38); etching at least a portion of said top surface with an etchant which preferentially attacks said first material (12) so as form a new top surface with said elements of said second material (14) protruding from surrounding portions of said new top surface (column 2, lines 1-2; column 3, lines 1-4). Moreover, the second material (14) projects above the surrounding portions of the top surface by a protrusion height of about 100 nm to 140 nm (column 3, lines 8-11). Yu further teaches that the alignment mark is generated by a blanket deposition of conductive layer (21) over the surface to produce an edge with sufficient optical contrast (column 3, lines 12-16). The thickness of conductive layer (21) is between 3,000 Å and 8,000 Å (column 3, lines 18-20), or a thickness less than about ten times the protrusion height. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form said metallic layer is less than about 500 nm thick. One who is skilled in the art would be motivated to form the lower additional layer with a sufficient thickness to produce sufficient optical contrast.

41. Claims 13-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of Zhou et al. (U.S. Patent No. 5,926,720).

42. As to claim 13, although Shih discloses said raised features are defined by said protruding second material elements (column 5, lines 4-14), the reference does not

expressly disclose that said one or more additional layers consist solely of transparent layers and wherein said locating step includes directing light through said transparent layers to said protruding second material elements. Zhou teaches that for conventional alignment of mask layers, if two features on non-successive layers require alignment, it is desirable to use a transparent intermediate layer, so that alignment marks in the underlying layer can be optically detected by bright field or dark field (column 1, lines 43-54). Moreover, Zhou teaches that a metal layer is typically covered by a transparent oxide layer (column 1, lines 55-59). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form one or more additional layers consist solely of transparent layers and wherein said locating step includes directing light through said transparent layers to said protruding second material elements. One who is skilled in the art would be motivated to use conventional mask alignment techniques.

43. As to claim 14, although Shih discloses depositing a layer of photoresist (column 5, line 18), the reference does not expressly disclose depositing one or more additional layers include depositing a transparent dielectric layer and then depositing a layer of a photoresist. Shih teaches forming a layer of photoresist (25) in order to pattern the electrode metal (column 5, lines 30-34). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to depositing one or more additional layers include depositing a transparent dielectric layer and then depositing a layer of a photoresist. One who is skilled in the art would be motivated to use

conventional mask alignment techniques and to pattern the metal electrode using photoresist.

44. As to claim 16, Zhou discloses that the said transparent dielectric layer includes an oxide (column 1, lines 55-59).

45. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of Allman et al. (U.S. Patent No. 6,136,662).

46. As to claim 19, Shih does not expressly disclose that said raised features form a diffraction grating and said step of detecting light includes detecting light diffracted by said grating. Allman teaches a common method of wafer alignment using diffraction gratings etched into the silicon, in which alignment is performed by collecting and processing first order spots from each of the diffraction gratings (column 1, lines 35-45). Moreover, Allman teaches that the diffraction grating is a series of parallel structures (Figure 2). Shih further discloses that alignment lines (14) are square (column 4, lines 13-15) and thus the protrusions formed by the etching step are parallel. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate raised features to form a diffraction grating and detecting light diffracted by the grating. One who is skilled in the art would be motivated to use a common alignment technique such as diffraction grating and to modify Shih's alignment lines to produce the appropriate grating.

47. Claims 15 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of Zhou, in further view of Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press (1986).

48. As to claim 15, Shih does not expressly disclose that said step of depositing one or more additional layers further includes depositing an antireflection coating on said transparent dielectric layer before depositing said photoresist. Wolf teaches that anti-reflective coatings are used to absorb the radiation that penetrates the photoresist, thereby suppressing standing waves and reducing scattering effects. Moreover, the coating also partially planarizes the wafer topography (page 441). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to depositing an antireflection coating on said transparent dielectric layer before depositing said photoresist. One who is skilled in the art would be motivate to improve lithography resolution by suppressing standing waves and reducing scattering effects.

49. As to claim 34, Shih discloses a method of processing a semiconductor wafer comprising the steps of: providing a starting wafer (10) (column 2, line 8) including a top layer of dielectric (12) with elements (32/34) therein, said layer having a planar top surface, said dielectric and said elements being exposed at said top surface (column 4, lines 47-55; Figures 7A-7B); etching said top surface with an etchant which preferentially attacks said dielectric (12) so as to leave said top surface with said elements (32/34) protruding from said dielectric (12) (column 5, lines 4-14); locating said elements by directing light and detecting light which has interacted with said elements, and registering the wafer with processing equipment based at least in part upon the locations of the elements (column 5, lines 27-44).

50. Shin does not expressly disclose polysilicon elements or a nitride dielectric. However, Shin teaches the general concept of exploiting the different etching

characteristics for elements (32/34) embedded in a dielectric (12), in order to form a protrusion, which is readily detectable as an alignment marker. Wolf teaches that silicon nitride is commonly used dielectric for semiconductor applications (page 191) and polysilicon is a commonly used conductor (page 176-77). Moreover, wet etching of silicon is typically performed with hydrofluoric and nitric acid (page 531). Wet etching of silicon nitride is performed with phosphoric acid (page 534). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the elements of polysilicon and the dielectric of silicon nitride. One who is skilled in the art would be motivated to use conventional dielectric or conductive materials. Moreover, one who is skilled in the art would be motivated to use two materials with different etching characteristics such that a protrusion may be readily formed as an alignment marker.

51. Shin does not expressly disclose depositing a transparent oxide layer on said top surface so that said polysilicon elements project into said oxide layer. However, Zhou teaches that for conventional alignment of mask layers, if two features on non-successive layers require alignment, it is desirable to use a transparent intermediate layer, so that alignment marks in the underlying layer can be optically detected by bright field or dark field (column 1, lines 43-54). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a transparent oxide layer on said top surface so that said polysilicon elements projects into said oxide layer. One who is skilled in the art would be motivated to use conventional mask alignment techniques. Moreover, one who is skilled in the art would also adapt any

subsequent photolithography process to account for the presence of the transparent oxide layer.

52. As to claim 35, Shih discloses depositing a photoresist before said locating step (column 5, lines 24-26).

53. As to claim 36, Shih discloses that said elements protrude above said dielectric layer by a protrusion height less than about 100 nm (column 5, lines 4-7).

Conclusion

54. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tseng (U.S. Patent No. 5,783,490) discloses a method of forming an alignment mark be forming step by etching a dielectric surrounding a metal plug.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
April 28, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER